Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A method for implementing a plurality of encoders and/or decoders (codecs) using a single digital signal processing (DSP) device, wherein the function of each codec is performed by the DSP according to an instruction code program, the method comprising the steps of:

providing an instruction code program stored in a first memory for controlling the DSP to function as a codec;

providing a second memory including a plurality of memory segments; and

implementing a plurality of codecs using the DSP by running said instruction code program in said first memory a plurality of times in re-entrant instances, wherein each codec instance is provided access to a respective separate memory segment in said second memory for storing data used in encoding/decoding a respective separate data stream.

2. (Original) The method of claim 1, wherein a third memory is provided which is accessible by each of the codec instances for shared storage of temporary variables and data buffering in encoding/decoding said respective separate data streams.

3. (Previously Presented) The method of claim 1, wherein each codec instance accesses the corresponding memory segment using indirect addressing based on at least one index register, the at least one index register being set for each

codec instance to modify addressing of variables for that codec instance to the corresponding memory segment.

4. (Original) The method of claim 3, wherein the plurality of memory segments are contiguous in said second memory, and said at least one index register is set for each codec instance according to an offset based on the difference in address from a first of said memory segments to the memory segment corresponding to that codec instance.

5. (Previously Presented) The method of claim 1, wherein each of the memory segments in said second memory is the same size.

6. (Previously Presented) The method of claim 1, wherein said first memory is provided with a plurality of instruction code programs for implementing different kinds of codecs, and wherein different codec instances may be selected from the different kinds of codec.

7. (Original) The method of claim 6, wherein each of the memory segments in said second memory is the same size, and the size of the memory segments is selected according to the maximum memory required by any of the plurality of different kinds of codec.

8. (Original) A data coding and/or decoding system in which a plurality of encoders and/or decoders (codecs) are implemented using a single digital signal processing (DSP) device, comprising:

a digital signal processor (DSP);

a first memory coupled to the DSP and containing an instruction code program, the function of each codec being performed by the DSP, in use, according to said instruction code program; and

a second memory coupled to the DSP and partitioned to include a plurality of separate memory segments;

wherein a plurality of codecs are implemented using the DSP by running said instruction code program in said first memory a plurality of times in re-entrant instances, and wherein each codec instance is provided access to a respective separate memory segment in said second memory for storing data used in encoding/decoding a respective separate data stream.

9. (Original) The system of claim 8, including a third memory coupled to said DSP which is accessible by each of the codec instances for shared storage of temporary variables and data buffering in encoding/decoding said respective separate data streams.

10. (Previously Presented) The system of claim 8, wherein each codec instance accesses the corresponding memory segment using indirect addressing based on at least one index register, the at least one index register being set for each codec instance to modify addressing of variables for that codec instance to the corresponding memory segment.

11. (Original) The system of claim 10, wherein the plurality of memory segments are contiguous in said second memory, and said at least one index register is set for each codec instance according to an offset based on the difference in address from a first of said memory segments to the memory segment corresponding to that codec instance.

12. (Previously Presented) The system of claim 8, wherein each of the memory segments in said second memory is the same size.

13. (Previously Presented) The system as claimed in claim 8, wherein said first memory is provided with a plurality of instruction code programs for implementing different kinds of codecs, and wherein different codec instances may be selected from the different kinds of codec.

14. (Original) The system of claim 13, wherein each of the memory segments in said second memory is the same size, and the size of the memory segments is selected according to the maximum memory required by any of the plurality of different kinds of codec.

15. (Original) A method for implementing a plurality of encoders and/or decoders (codecs) using a single digital signal processing (DSP) device, wherein the function of each codec is performed by the DSP according to an instruction code program, the method comprising the steps of:

providing an instruction code program stored in a first memory for controlling the DSP to function as a codec;

providing a second memory including a plurality of memory segments; and

implementing a plurality of codecs using the DSP by running said instruction code program in said first memory a plurality of times in re-entrant instances, wherein each codec instance is provided access to a respective separate memory segment using an indirect addressing mode based on at least one index register in said second memory for storing data used in encoding/decoding a respective separate data stream.

16. (Original) A data coding and/or decoding system in which a plurality of encoders and/or decoders (codecs) are implemented using a single digital signal processing (DSP) device, comprising:

a digital signal processor (DSP);

a first memory coupled to the DSP and containing an instruction code program, the function of each codec being performed by the DSP, in use, according to said instruction code program; and

a second memory coupled to the DSP and partitioned to include a plurality of separate memory segments;

wherein a plurality of codecs are implemented using the DSP by running said instruction code program in said first memory a plurality of times in re-entrant instances, and wherein each codec instance is provided access to a respective separate memory segment using an indirect addressing mode based on at least one index register in said second memory for storing data used in encoding/decoding a respective separate data stream.

17. (New) The system of claim 16, including a third memory coupled to said DSP which is accessible by each of the codec instances for shared storage of temporary variables and data buffering in encoding/decoding said respective separate data streams.

18. (New) The system of claim 16, wherein each of the memory segments in said second memory is the same size.

19. (New) The method of claim 15, wherein a third memory is provided which is accessible by each of the codec instances for shared storage of temporary variables and data buffering in encoding/decoding said respective separate data streams.

20. (New) The method of claim 15, wherein each of the memory segments in said second memory is the same size.